AMENDMENTS TO THE CLAIMS

Please amend the claims as set forth in the following listing. This listing of claims will replace all prior versions, and listings, of claims for the present application:

Claims 1-54 (Canceled).

55.(Currently Amended) A process for using a photo-definable layer in a negative mask scheme to manufacture a semiconductor device, comprising:

forming over a substrate a photo-definable layer that is convertible to an insulative material;

exposing selected portions of said photo-definable layer to electro-magnetic radiation in a negative pattern scheme to convert said selected portions to an insulative material;

removing non-exposed portions of said photo-definable layer with an etch process that is selective to exposed portions of said photo-definable layer;

using said exposed portions of said photo-definable layer as a patterned etch mask for further processing steps, and

leaving said exposed portions of said photo-definable layer as an insulative layer within said semiconductor device.

56.(Previously Presented) The process of claim 55, wherein said photo-definable layer comprises an organosilicon resist.

57. (Previously Presented) The process of claim 56, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

58. (Previously Presented) The process of claim 57, further comprising converting said PPMSO layer to oxide through exposure to an oxygen plasma.

59.(Currently Amended) A semiconductor device formed using a photo-definable layer in a negative mask scheme, comprising:

a substrate;

at least one feature formed on said substrate by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a

negative mask scheme, by using exposed portions of said photo-definable layer as an etch mask to form said at least one feature, and by leaving said exposed portions of said photo-definable layer on said substrate as an insulative layer.

60. (Previously Presented) The semiconductor memory device of claim 59, wherein said photo-definable layer comprises an organosilicon resist.

61. (Previously Presented) The semiconductor memory device of claim 60, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

Claims 62-75 (Canceled).

76. (Currently Amended) A process of using a photo-definable layer in a Damascene process to create a patterned structure, comprising:

forming on a substrate a photo-definable layer that is convertible to an insulative material;

exposing selected portions of said photo-definable layer to electro-magnetic radiation to convert said selected portions to an insulative material;

removing non-exposed portions of said photo-definable layer with an etch process that is selective to exposed portions of said photo-definable layer to form a desired pattern within said exposed portions of said photo-definable layer; ~~and~~

leaving said exposed portions of said photo-definable layer on said substrate as an insulative layer~~.~~; and

converting said insulative layer to an oxide layer through exposure to an oxygen plasma.

77. (Previously Presented) The process of claim 76, wherein said photo-definable layer comprises an organosilicon resist.

78. (Previously Presented) The process of claim 77, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS) and said insulative material comprises photo-oxidized siloxane (PPMSO).

79. (Currently Amended) The process of claim 78, further comprising ~~converting said PPMSO to an oxide layer by exposure to oxygen plasma and~~ consolidating said oxide layer with an anneal.

80. (Previously Presented) The process of claim 79, further comprising depositing a conductive material within said pattern.

81. (Previously Presented) The process of claim 80, wherein said conductive material forms an interconnect structure within a semiconductor memory device.

82. (Previously Presented) The process of claim 76, wherein said exposing step is performed by irradiating said selected portions of said photo-definable layer with ultraviolet light in the presence oxygen.

83. (Previously Presented) The process of claim 82, wherein said non-exposed portions of said photo-definable layer are removed using a chlorine-based or a bromine-based plasma etch.

84.(Previously Presented) A conductive interconnect structure within a semiconductor device formed using a photo-definable layer, comprising:

a substrate;

a patterned insulative layer on said substrate formed by converting selected portions of a photo-definable layer to an insulative material through exposure to electro-magnetic radiation in a negative mask scheme, by removing non-exposed portions of said photo-definable layer to form a pattern within said photo-definable layer, and by leaving said exposed portions of said photo-definable layer as said patterned insulative layer; and

a conductive layer inlaid within said patterned insulative layer.

85. (Previously Presented) The semiconductor structure of claim 84, wherein said photo-definable layer comprises an organosilicon resist.

86. (Previously Presented) The semiconductor structure of claim 85, wherein said photo-definable layer comprises plasma polymerized methylsilane (PPMS).

87. (Previously Presented) The semiconductor structure of claim 84, wherein said conductive layer forms an interconnect structure within a semiconductor memory device.

Claims 88-100 (Canceled).